

Abdullah B. Kaykha  
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## ACCOMPLISHMENTS SUMMARY

- Managed and oversaw multiple projects throughout design process and remanufacturing custom- and semi-designed switching mode power supplies, planned their production process, purchased materials, and reduced material cost by over 30%.
- Coordinated manufacturing and assisted engineering manager and design group in building simple to moderately complex prototypes as well as providing step by step manufacturing instructions such as sequence of events (SOE), quality inspection checklist, and test procedures thereby reducing labor cost.
- Gained good understanding of process and hands on with major process tools and metrology / test equipment performing process engineering functions in a class 1000 clean room.
- Performed product demo on Lam Research etchers and conducted hardware development and CIP projects as a Process R & D Engineer.
- Co-authored a publication in the Proceedings American Ceramic Society, 1992 for a project at NASA Ames, CA "A Study of the Co-deposition of TiCl<sub>4</sub>, BCl<sub>3</sub> and Dimethyl-dichlorosilane (DDS) on Carbon in a Hot-wall Tubular Reactor".
- Wrote technical papers and provided technical support.

## SKILLS

- **Process and Metrology Equipment:** Deposition Furnaces, Thin Film Deposition tools, Reactive Ion Etcher, SVG Track, Perkin Elmer Aligner; optical microscope, Nanospec, Scanning Electron Microscope (SEM), FTIR, Four Point Probe.
- **Electronics Testing Equipment:** Digital multi-meter (DMM), signal generator, oscilloscope, curve-tracer, variable DC power supply, AC and DC hi-pot tester, Logic Analyzer, Quad Electronics load unit.
- **Personal Computer:** Integration and upgrades, Windows installations and administration, networking and internet setup, web server setup, MS Office, OrCAD Capture and Layout, Multisim, Xilinx Foundation Simulation, AutoCAD.
- **Other:** Excellent communication and organizational skills; reliable, dedicated, and self motivated; DOE and SPC

## EDUCATION

B. S. Materials Engineering, San Jose State University, San Jose, CA

## EXPERIENCE

### **Production & Regulatory Compliance Engineer**, ETA – USA, Morgan Hill, CA 2000 – 2002

Managed and oversaw multiple projects pertaining to the manufacturing of special purpose custom- and semi-designed switching mode power supplies, and planned their production process; interfaced with UL field service representatives and took corrective actions to resolve UL safety issues; utilized OrCAD Capture and Layout for PCB (printed circuit board) layout; coordinated with and assisted design engineers in building simple to moderately complex prototypes; performed numerous electrical measurement tests for quality validation and UL safety approval.

### **Applications Engineer**, SITE Services, Inc., Santa Clara, CA 1998

Conducted presentations and demonstrated Millennium 2000 photolithography pick-and-place (track system) process stations to potential customers, tested process modules, and wrote technical papers.

### **Process Engineer**, Universal Semiconductor, Inc., San Jose, CA, 1996 – 1997

Sustained various areas of fab such as photolithography, etch, and furnaces; and assisted in projects such as "dielectric isolation" (DI) wafers for HVDMOS.

### **Process Engineer**, Lam Research Corp., Fremont, CA 1995 – 1996

Worked in Tungsten Etch Technology R & D Division performing demos and process development on Lam Rainbow 4720; characterized process by SEM and four-point probe; applied design of experiments (DOE); wrote technical papers and made presentations on demos and projects.

### **Manufacturing Engineer**, Adaptive Electronics & Adaptive Systems, San Jose, CA 1994 – 1995

Coordinated various groups of manufacturing, layout, and design involved in the production of customized burn-in systems, burn-in boards and other boards (drivers, power supplies, controllers, and pattern-generators), and subassemblies; resolved production issues; coordinated BOMs entries, supervised test technicians, assemblers, and purchasing departments.

### **Manufacturing Engineer (Temp)**, Silicon Valley Group, Inc., San Jose, CA 1993 – 1994

Supported the design and manufacturing of SVG track systems; wrote specifications for and supported Final Test and Source Inspection Groups (QA); wrote SOEs and ECOs.